QUIZ COE223

· Doing 3-bit left logical shift:

1) Divides the number by 2
2) Divides the number by 4
3) Multiples the number by 8
4) Multiples the number by 4

· Doing 2-bit right arithmetic shift:

1) Divides the number by 2
2) Divides the number by 4
3) Multiples the number by 2
4) Multiples the number by 4

· What is the delay for the following types of 64-bit adders? Assume that each two-input gate delay is 150 ps and that a full adder delay is 350 ps.

a) Prefix :

$$t_{PA} = t_{pg} + log_2 N \left(t_{pg_prefix}\right) + t_{XOR}$$

$$150 + log_2 64\big(2(150)\big) + 150$$

150 + 6 (300) + 150

150 + 1800 + 150

= 2100ps

= 2100 ÷ 1000 = 2.1ns

QUIZ COE223

· Doing 1-bit left logical shift:

1) Divides the number by 2
2) Divides the number by 4
3) Multiples the number by 2
4) Multiples the number by 4

· Doing 3-bit right arithmetic shift:

1) Divides the number by 2
2) Divides the number by 8
3) Multiples the number by 2
4) Multiples the number by 4

· What is the delay for the following types of 32-bit adders? Assume that each two-input gate delay is 200 ps and that a full adder delay is 300 ps.

a) Prefix :

$$t_{PA} = t_{pg} + log_2 N \left(t_{pg_prefix}\right) + t_{XOR}$$

$$200 + log_2 32\big(2(200)\big) + 200$$

200 + 5 (400)+200

200+2000+200

= 2400ps

= 2400÷1000 =2.4ns

QUIZ COE223

· Which type of shift would lose the sign of a negative number ?

1) Left logical shift
2) Right logical shift
3) Right arithmetic shift
4) None

· Doing 1-bit right arithmetic shift:

1) Divides the number by 2
2) Divides the number by 4
3) Multiples the number by 2
4) Multiples the number by 4

· What is the delay for the following types of 32-bit adders? Assume that each CLA has 4-bit blocks, two-input gate delay is 300 ps and that a full adder delay is 200 ps.

a) CLA :

$$t_{CLA} = t_{pg} + t_{pg_block} + (N/k - 1)t_{AND_OR} + kt_{FA}$$

$$300 + (2(4) - 2)300 + (32/4 - 1)2(300) + 4(200)$$

300 + 1800 + 4200 + 800

= 7100ps

= 7100 ÷ 1000 =7.1ns